A Low-Power 65nm CMOS Ultra-Wideband Low-Noise Amplifier for 12 – 16GHz Communications

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***Abstract*—This paper presents a 65-nm CMOS low-noise amplifier (LNA) with an ultra-wideband (UWB) frequency range of 12 – 16GHz. A two-stage amplifier topology is used, where the first stage matches the input to 50Ω over the frequency range, while the second stage uses a cascode configuration to gain the signal. The single-ended circuit has low power consumption and low area. It has a power gain greater than 10dB, input matching under -10dB, and reverse isolation under -47dB in the 12 – 16GHz range. It draws 13.9mA from a 1.2V power supply.**

Keywords— CMOS, low-noise amplifier (LNA), ultra-wideband (UWB), low-power amplifier;

I. Introduction

The Ku-Band encompasses the 12 – 18GHz portion of the electromagnetic spectrum. It is used mainly for satellite communications, including television and internet. It is also used by NASA for communication with space shuttles and the International Space Station. The band extends from 12 to 18GHz, but most federal and commercial uses only go up to 16GHz. Systems that transmit wireless data over these frequencies integrate a low-noise amplifier (LNA) followed by a down-conversion mixer which is fed by a voltage-controlled oscillator. In these systems, it is critical for the LNA to have good input matching and a low noise figure (NF) over the entire receiving band. It is also desirable to have low power consumption and small silicon layout area.

A two-stage ultra-wideband (UWB) LNA design targeted for use in the 12 – 16GHz spectrum is presented in this paper. An UWB LNA has a large bandwidth, which allows for high data rates in wireless communication. This UWB LNA features two stages: a complementary amplifier stage with source degeneration, and a cascode amplifier stage with a low-Q resonant load. It provides good impedance matching and low NF over the frequency band. The UWB LNA is built, simulated, and laid out with Cadence software using a TSMC 65nm technology node.

This paper discusses various UWB LNA topologies and the design procedure for the topology selected. The circuit schematic is shown and results of the simulations are presented. An explanation of the silicon layout is also given. Finally, the circuit performance is compared to other existing LNAs.

II. Discussion of UWB LNA Topologies

A. Performance Requirements of LNAs

A well-performing UWB LNA must have good noise matching, high reverse isolation, low NF, and high gain over the targeted receive band. 50Ω input noise matching and high reverse isolation are important because they prevent the received signal from being reflected back towards the antenna, which causes undesired wireless noise. Having a low NF is essential because the LNA is the first stage in an integrated receiving system, so its noise is cascaded through all the following stages of the system. A combination of low NF and high gain in the LNA stage will allow the receiver to have good sensitivity. Also, an LNA that uses a simple topology with few components and low current consumption is desirable because it will reduce the on-chip area needed to implement passive components while maintaining a small power budget. To this end, single-ended LNAs are preferable to differential LNAs because they need half the amount of components and current consumption, and do not require baluns.

B. UWB LNA Topologies

There are various CMOS topologies that are used to implement UWB LNAs. Figure 1 (taken from [1]) shows five topologies that are commonly used.

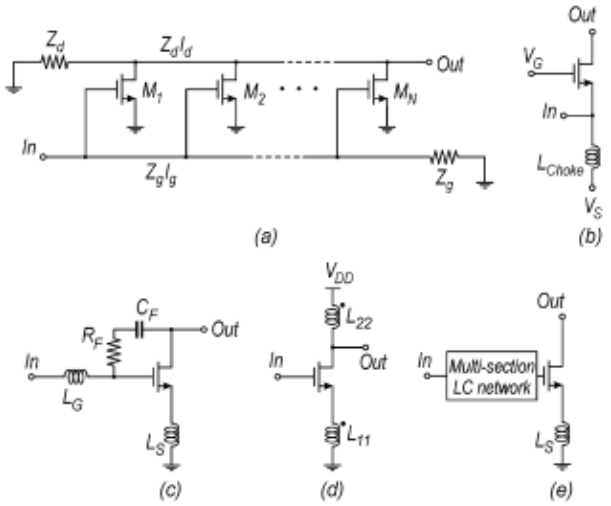

Fig. 1: UWB LNA topologies – a) distributed LNA, (b) common gate, (c) resistive feedback, (d) reactive feedback, and (e) multisection reactive network

The distributed amplifier shown in 1(a) uses multiple tuned loads to have a flat gain and matching over a wide bandwidth, but requires a large amount of chip area. A common gate amplifier, as shown in 1(b), has an input impedance dependent on the gain of the transistor, which can be used to have a matched input over wide bandwidth. Resistive and reactive feedback LNAs such as those depicted in 1(c) and 1(d) have good gain and noise matching. However, the resistive feedback adds thermal noise, while the reactive feedback requires large on-chip inductors. Another common topology is a noise-cancelling topology where the noise is canceled out by adding

a negatively gained signal to the desired signal, such that the noise is subtracted out. An amplifier with a low-Q resonant load can also be used as a UWB LNA, but it is difficult to get good noise performance while having a low enough Q to get flat gain over a large bandwidth.

III. 12 – 16GHz UWB LNA Design

A. Topology

The UWB LNA is be implemented using a two-stage single-ended topology derived from IEEE TMTT paper "A 3-10 GHz Low-Power CMOS Low-Noise Amplifier for Ultra-Wideband Communication" [1]. The general circuit design is shown in Figure 2.

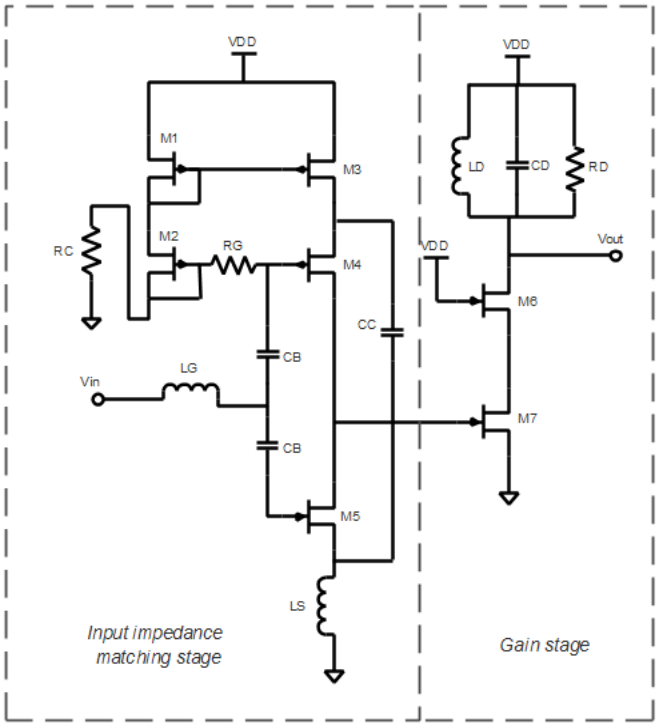

Fig. 2: Two-stage UWB LNA

The first stage of the LNA uses a single-ended complementary amplifier. The primary purpose of the first stage is to match the input impedance to 50Ω over the desired range of frequency. This is accomplished by establishing two resonant frequencies for the input impedance. The first frequency is set by LG, LS, and CGS of the MOSFETs. The second resonant frequency is set by LS and the capacitances present at node S. The effective CGD of the MOSFETs changes with the first-stage gain due to the Miller Effect. As the frequency changes, the gain changes, so the Miller Effect can be used to help keep the input matched to 50Ω over the wide band. Noise and impedance matching are optimized by selecting proper inductor and device sizes.

The second stage of the amplifier contributes high gain over the 12 – 16GHz range. A relatively flat gain over the band is achieved by tuning the R-L-C load to the upper portion of the range. RD reduces the Q-factor of the resonant load, so it has a flatter and wider gain over the frequency range.

An operational transconductance amplifier is used in [1] along with cascode current mirrors to bias the input stage. In this design, only the PMOS cascade current mirrors are used to bias the input stage.

This topology has several advantages. It is single-ended, so it has low power consumption and does not require a balun at the input. The matching of the first stage allows the amplifier to have low S11 over the wide frequency band. Having two stages significantly reduces the reverse isolation, S12.

B. Design Process

The component values were selected using equations given in [1]. The MOSFET widths in the first and second stage were selected to obtain a near-peak gm for a given bias current. L_G and L_S were calculated to obtain 50Ω matching impedance and a resonant point close to 14GHz. L_D and C_D of the resonant load were calculated to obtain a resonant point close to 15GHz, which is in the upper part of the band as recommended by [1]. Large capacitances were used for the blocking capacitors C_B and C_C, but not so large that they would be difficult to implement in the silicon layout.

After calculating initial values for the components, the circuit is simulated in Cadence and tweaked to obtain the desired performance. The resonant frequency of the first stage is heavily sensitive to the C_{GS} of M5, so the width of M5 was swept to determine the best size. The values of L_G and L_S were adjusted to have a better wide-band input matching.

IV. Silicon Layout

The layout of the UWB LNA is shown in Figure 3.

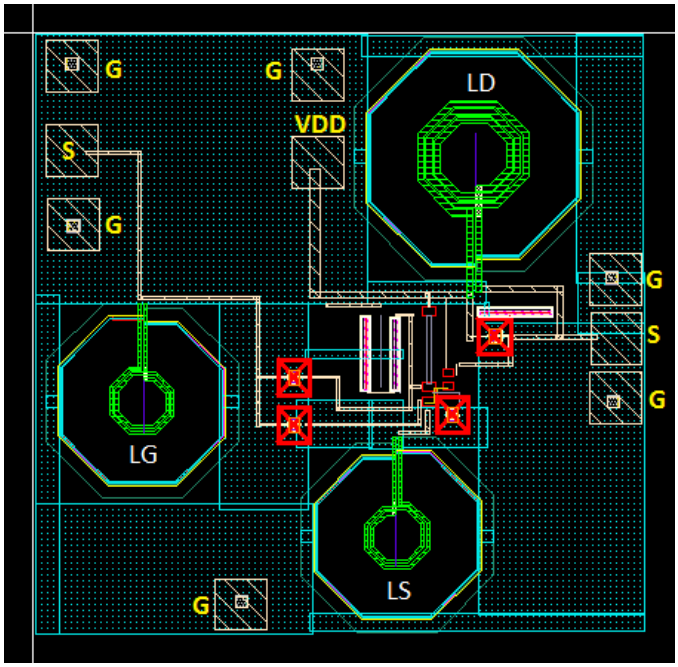

Fig. 3: Layout of UWB LNA

The input and output signal pads are each neighbored by two ground pads to provide a 50Ω characteristic impedance interconnect. The signal path through the two amplifier stages

is routed on wide wires to maintain a 50Ω characteristic impedance transmission line. The traces connecting to VDD are made wide to support the large amount of DC bias current flowing on them. The inductors are implemented using spiral traces on the top metal layer with large guard rings around them to reduce parasitic capacitance. The capacitors are implemented as MIMCAPs from the TSMC RF library.

The Metal 1 layer was used as a ground plane for the entire circuit. All of the signal traces are routed over the ground plane to help maintain the characteristic impedance. There is no ground plane underneath the active devices or the inductors. The ground plane is plugged in to each of the input GND pads using via stacks.

V. Simulation Results

The simulation results are shown in Figures 4 – 7.

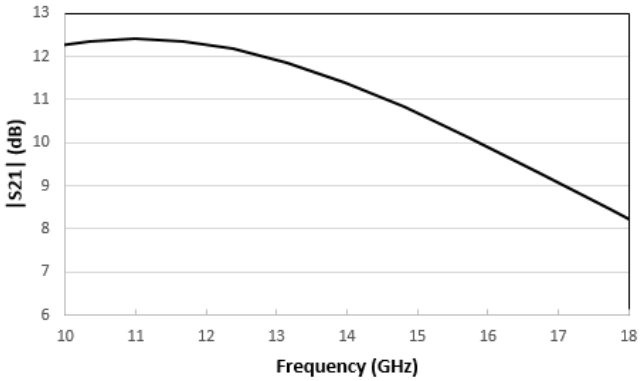

Fig. 4: Simulated $|S_{21}|$

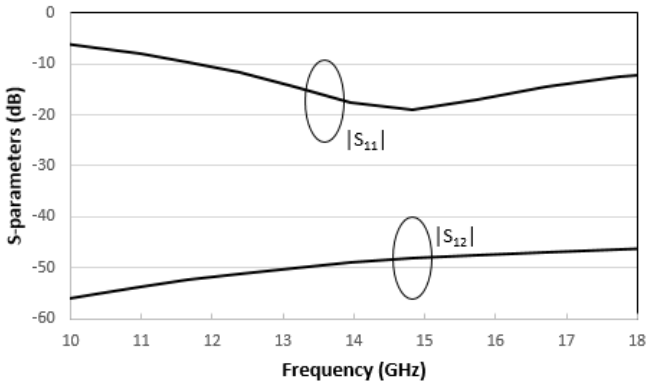

Fig. 5: Simulated $|S_{11}|$ and $|S_{12}|$

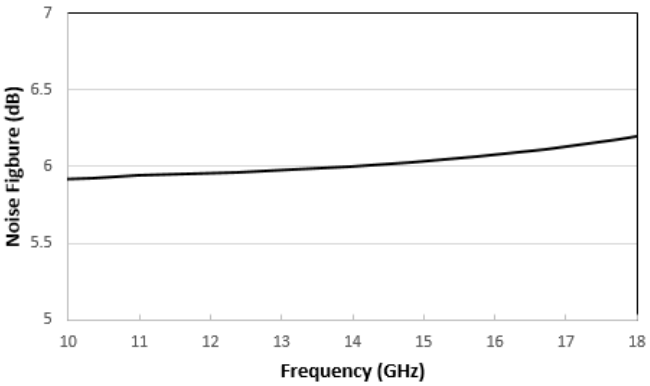

Fig. 6: Simulated NF

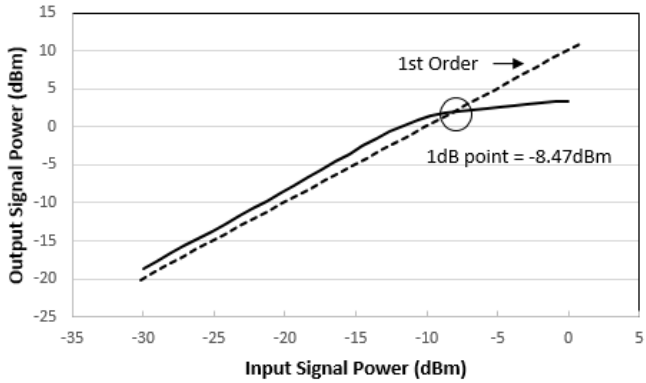

Fig. 7: Simulated Input Referred 1dB Compression Point

The $|S_{21}|$ magnitude peaks around 11GHz, which is outside of the targeted range, but still maintains a relatively flat and high gain of 12.2 – 10dB from 12 – 16GHz. The peak frequency is mainly set by C_{GS} of M5, and is easily adjustable. However, it was observed that better gain could be achieved by having the resonant frequency around 11GHz than if it were between 12 – 16GHz.

$|S_{11}|$ has a minimum point at 14.7GHz, and increases rather sharply from there. This indicates that the input matching circuit is heavily tuned to one frequency rather than the targeted 12 – 16GHz band. However, it still remains beneath -10dB from 12 – 16GHz. The results for $|S_{12}|$ show that the LNA has excellent reverse isolation, as it is beneath -47dB at frequencies lower than 16GHz.

The simulated NF is 6 ± 0.05 dB from 12 – 16GHz. It remains flat and constant through the target receiving band. The simulated input referred 1dB compression point is -8.57dBm. This indicates that the LNA has considerably linear behavior. The circuit draws 13.9mA from the 1.2V power supply.

Table 1
Performance Comparison Between Similar Works

TECHNOLOGY NODE	RECEIVE BAND (GHZ)	NF (DB)	S_{11} (DB)	S_{21} (DB)	S_{12} (DB)	$IP1_{DB}$ (DBM)	P_{DC} (MW)	V_{DD} (V)	CHIP AREA (MM^2)	REFERENCE
90-nm CMOS	2.6 - 10.2	3 - 7	-9	12.5	-45	-12	7.2	1.2	0.64	[1]
0.18-µm CMOS	2.7 - 9.1	3.8 - 6.9	< -10	10	N/A	N/A	7	0.6	N/A	[2]
0.18-µm CMOS	1 - 5	2.6 - 3	< -7	21 - 25	N/A	N/A	14.5	N/A	N/A	[3]
0.18-µm CMOS	3.1 - 10.6	5.5	< -8.1	10.8	< -30.5	-6.4	6.4	N/A	0.97	[4]
90-nm CMOS	14.5	5.8 ± 0.2	< -10	10	N/A	-4 - 1	30	N/A	0.375	[5]
0.18-µm CMOS	3 - 14	4 - 1.5	< -11	14	N/A	-16	N/A	N/A	N/A	[6]
65-nm CMOS	**12 - 16**	**6 ± 0.05**	**< -10**	**12.2 - 10**	**< -47**	**-8.6**	**16.7**	**1.2**	**0.34**	**This work**

Table 1 shows a comparison of this work to other published UWB LNA topologies targeting similar frequency ranges. It was difficult to find other papers describing UWB LNAs specifically for the Ku-band frequencies, so other frequency ranges are compared. Overall, the LNA presented in this paper is comparable to those from other works. It has similar noise figure, impedance matching, and gain.

VI. Conclusion

A 12 – 16GHz UWB LNA designed for Ku-band receiver applications was presented in this paper. The design and operation of the circuit is discussed. A Cadence silicon layout is shown and simulation results from the circuit are presented. Overall, the circuit has good performance in its low NF and impedance matching. The circuit performance is comparable to other UWB LNAs published in recent works.

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