Rugged Data Logger

Evan Juras

4/12/2017

Abstract: The specifications, architecture, analog subsystem, PCB layout, and test plans are proposed for a rugged yet low cost data logger that can used for simple data acquisition in electromagnetic test setups or other electrically hostile environments.

Table of Contents

1. Summary

The Rugged Data Logger is a general-purpose analog acquisition system made for logging transduced signals (such as battery charger current or controller voltages) during electromagnetic compatibility (EMC) testing or other harsh electric transient conditions. It is designed to be low cost and easily usable while still being able to withstand electrical interference (EMI) that occurs during EMC tests or field usage of industrial equipment such as motor controllers or substation relays. It has a signal bandwidth of 1.5kHz and an input range of ±1V.

The proposed hardware specifications, architecture, analog subsystem, PCB layout, and test plan for the data logger are presented in this document.

2. Hardware Specifications

A. Design Requirements

The data logger shall meet the following requirements:

- The data logger is a standalone device that has a power input, a single differential analog input (signal and return wire pair), and a communications port to access the data
- Measurement data shall be locally stored and have enough storage memory to hold 24 hours of data
- The incoming analog signal must be converted to 14-bit digital values at a 10kHz sample rate
- Accept an input signal range of ±1V
- Powers itself off an input power supply voltage ranging from 18 – 36VDC
- The data logger must be isolated from the input power supply
- Have an average power consumption of 500mW maximum

B. Additional Design Objectives

The data logger will also be designed to meet the following objectives:

- Analog signal bandwidth of 1.2kHz, and ≥ 10dB of attenuation at 5kHz (the frequency at which aliasing begins to occur)
- Able to withstand harsh EMI events such as radiated and conducted high frequency interference and electrical transients
- Small form factor to allow it to be used in space-constrained applications
- -40°C to 85°C temperature range to allow it to be used in a wide variety of environmental conditions
- Low cost
- 10-year product lifetime

3. Architecture Block Diagram

A block diagram of the data logger architecture is shown in Figure 1.

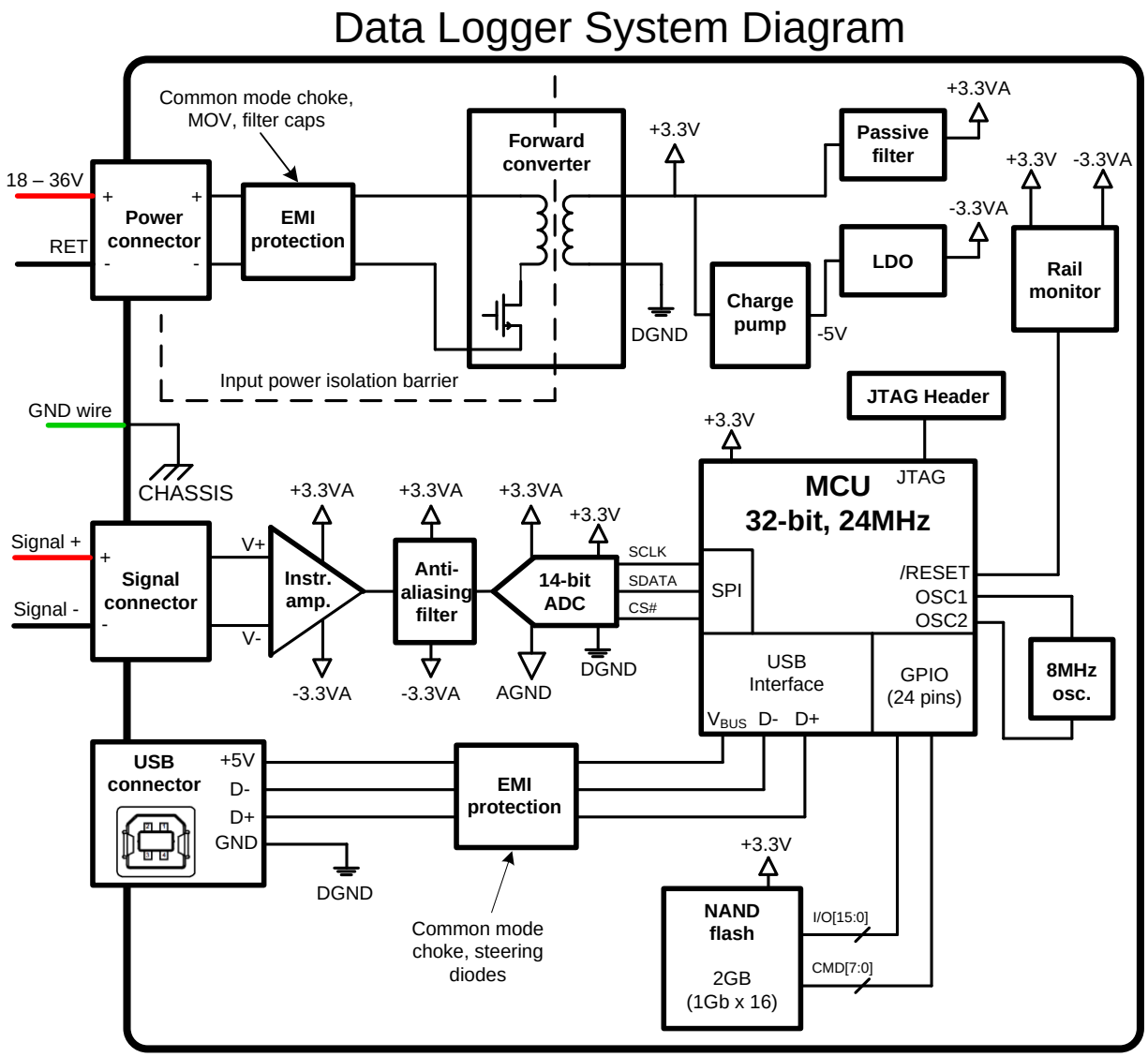


Figure 1. Data logger architecture

The analog signal pair is landed on a connector, routed through the analog front-end, and converted to a 14-bit digital value by an ADC operating at a sample rate of 10kSPS. The 14-bit samples are transmitted to a microcontroller (MCU) through an SPI interface. The MCU collects sample data in temporary internal SRAM and then writes it to permanent external NAND flash storage. A USB interface is used to access and download the data on a separate device. Input power is isolated and stepped down using a forward converter to generate the +3.3V rails that power all the devices on the board.

The following sections describe each subsystem of the block diagram. Some sections also give an analysis verifying that the architecture meets the requirements given in Section 2.A.

A. Microcontroller (MCU)

Primary MCU functions:

- Control the 10kHz sample rate of the ADC
- Collect 14-bit samples from the ADC and store them in internal SRAM
- Write data from SRAM to NAND flash
- Download data to an external device through the USB interface

Data acquisition and storage:

When the MCU's SRAM collects 4KB worth (the size of one page of NAND flash) of samples from the ADC, the MCU begins writing the 4KB to a page of NAND flash. While writing to flash, it continues acquiring ADC samples and storing them in SRAM. When the write to flash is complete, it resets to the beginning of the 4KB SRAM data block and begins overwriting old data with new data. This allows the MCU to continuously acquire samples while writing them to flash 4KB at a time.

Interfaces:

The MCU interfaces to the ADC through a 3-wire SPI interface. It connects to the NAND flash through a 24-bit interface (16 I/O lines and 8 command/status lines). It connects to an external device through a USB interface that allows data to be accessed. An 8MHz external reference oscillator is used because it is required by the USB interface to meet timing. The MCU also has a JTAG interface that allows for firmware downloading and debugging.

MCU specifications:

Specifications for the MCU are given in Table 1.

Table 1 – MCU Specifications

Feature	Specification	Reason
Architecture	32-bit	Allows more flexibility in processing and interface options while having similar cost to a 16-bit architecture
CLK frequency	24MHz	Provides adequate throughput to acquire ADC samples and write to flash simultaneously, and to run USB interface
Internal SRAM	≥ 32KB	5KB is required for temporary ADC data, leaving 27 KB for program space, which will be enough for data logging routine
Internal flash	≥ 128KB	Provides enough code space to store entire data logging program
GPIO/data pins	≥ 24 pins	24 pins are needed to interface to the NAND flash
USB interface	Supported	Data will be accessed through external USB cable
SPI interface	Supported	ADC to MCU interface
JTAG interface	Supported	Allows firmware to be downloaded and debugged

MCU options:

Two MCU options that meet all of the above requirements are listed in Table 2.

Table 2 – MCU Options

Manufacturer	MFG Part Number	Cost per part (1k volume)
Microchip	PIC32MX250F256H-I/PT	$2.73
NXP	MKL26Z256VLH4	$2.75

The Microchip part is selected because the system was originally designed around this part.

B. NAND Flash

The 2GB NAND flash stores all ADC data.

Storage requirements:
The data logger has a unique requirement in that it must store at least 24 hours' worth of 14-bit, 10kSPS data. The total storage space required is calculated as 1.512GB:

$$\left(\frac{14\ bits}{sample}\right) * \left(\frac{1\ byte}{8\ bits}\right) * \left(\frac{10000\ samples}{1\ s}\right) * \left(\frac{60 s}{1\ min}\right) * \left(\frac{60 min}{1\ hr}\right) * 24 hr = 1.512 GB$$

NAND flash is selected as the data storage technology because it is cost-effective, it works well for storing sequential data, and it doesn't require a fast processor frequency. 2GB of storage is used because 1.5GB parts are uncommon and the extra space provides headroom for write-leveling and bad block management. A 16-bit wide interface is used because it is convenient for storing the 14-bit ADC samples.

Firmware must halt data acquisition when the flash is completely filled with data. The data must be erasable by a command from the USB device.

Assuming the flash is filled up and then erased once a day, it must have a PROGRAM/ERASE endurance of at least 3,650 cycles to support a product lifetime of 10 years. The firmware must implement bad block management and write leveling to maintain flash integrity.

Part selection:
The Micron MT29F16G16ADACAH4-IT part is selected. It has the following specifications:

- 2GB (8Gb x 16)
- Endurance: 60,000 PROGRAM/ERASE cycles
- Page size: 4KB
- Operating voltage: 1.8V or 3.3V
- Cost per unit (1k volume): $23.44

These specifications work well with the selected MCU and allow the data logger to meet the storage requirements given in Section 2.A. The part is high cost, but it is selected over using two 1Gb x 8, $6.52 parts in parallel to reduce PCB space and complexity.

C. USB Port

The USB port is a communication interface that allows an external device to connect and access or download data from the data logger.

Data throughput:
The USB communication interface is used because of its fast data transfer speed. The MCU datasheet specifies a maximum USB data throughput of 0.83MB/s. At this data rate, it will take 30 minutes to download the full 24 hours' worth of data (1.512GB):

$$1.512GB * \frac{1s}{0.83MB} * \frac{1min}{60s} = 30.36min$$

Slower communication interfaces would take considerably longer.

EMI protection:
The USB interface connects directly to the pins of the MCU, so the following components will be used to protect the MCU:

- Common-mode choke on D+ and D-: Attenuates any high-frequency noise that couples on to the USB cable.
- Steering diodes on D+ and D-: Conduct when signals are overvoltaged or undervoltaged, routing energy from electrostatic discharge or other electrical transients to the +5V rail or GND instead of to the MCU.

D. Analog Input

The analog signal chain conditions the input signal and passes it to an ADC, where it is converted to a 14-bit digital value. The full analog input schematic is included in Section 4.

Input instrumentation amplifier:
A Texas Instruments INA333 differential instrumentation amplifier (cost: $1.80) is used as the first block of the signal chain, providing the following advantages:

- Provides a high impedance input so the transducer producing the ±1V signal isn't loaded down
- Converts differential signal to single-ended so the differential pair doesn't have to be routed through the rest of the analog chain

The amplifier is powered by ±3.3V, giving it an input common mode range of -3.2V to 3.2V. The input ±1V signal has a maximum common mode voltage of ±0.5V, so it is within the input range of the amplifier. The amplifier is configured for a gain of 1, so the output voltage will be ±1V, which is within the -2.8V to 2.8V output range of the amplifier.

A passive RC filter with a corner frequency of 100kHz is used at the input to attenuate conducted RF noise, which can cause DC offset in the instrumentation amplifier.

Anti-aliasing filter:
A third-order Butterworth filter designed with a 1.2kHz corner frequency is used as an anti-aliasing filter for the analog input. It creates -13dB of attenuation at 5kHz, which is the Nyquist frequency for the 10kHz acquisition system. Simulations of the gain over frequency and transient stability of this filter are shown in Section 4.

The filter is implementing using an Analog Devices AD8651 op-amp (cost: $1.85). The unity-gain amplifier is powered by ±3.3V, so it has a high enough input and output voltage range to accommodate the ±1V signal.

ADC:
A Texas Instruments ADC141S626 ADC (cost: $2.75) is selected as the 14-bit ADC used by the data logger. It has a maximum sample rate of 250kSPS and a minimum sample rate of 50kSPS. The MCU will operate the ADC at 100kSPS and only store one of every ten samples to allow it to operate at 10kSPS. The ADC is differential, but one input will be grounded to use it in single-ended mode. The ADC is primarily selected for its low cost compared to other industrial-rated options.

A 1.024V, 0.1%, 50ppm reference voltage (Microchip MCP1501, cost: $0.58) is used for the ADC. This sets the nominal range of the ADC to -1.024V to +1.024V, giving it a LSB resolution of 125uV.

E. Power

The 18 – 36V power input is stepped down to +3.3V, which is used to power the MCU and flash. A +3.3V analog rail is created by filtering the +3.3V rail through a passive LC network. The primary +3.3V rail is fed to an inverting charge pump to generate -5V, which is passed through a filtering LDO to generate a -3.3V analog rail. The analog rails are used to power the devices in the analog input chain. The +3.3V and -3.3VA rails are monitored by an IC that asserts a system-wide /RESET if the rails go outside a ±5% tolerance band.

Topology:
A forward converter topology is used to step down the input voltage because it requires relatively low PCB area while providing isolation, thus meeting the requirement for the data logger to be isolated from the input power supply. The isolation barrier protects the device from high common mode voltages that can occur on the power inputs due to EMC events or ground differentials. A switch controller IC will be used to control the duty cycle of the FET and provide undervoltage and overvoltage lockout thresholds at 15V and 39V, respectively.

A 3.3V rail is the only voltage rail used because all components on the board are able to be powered by 3.3V. This reduces complexity of the board's power management and distribution.

Power analysis:
The datasheets power usage values for the major components on the board are shown in Figure 2. The power consumption of each part is added up to find total power usage. Then, it is assumed that the input power supply is 85% efficient overall, so the total power is divided by 0.85 to obtain the estimated input power.

Data Logger Power Estimate			
Part	VDD[1] (V)	Supply Current (mA)	Power (mW)
MCU[2]	3.465	12.00	41.58
NAND flash	3.465	35.00	121.28
Inst. Amp[3]	3.465	0.08	0.28
Op-amp[4]	3.465	15.50	53.71
ADC	3.465	1.15	4.00
Vref	3.465	0.26	0.90
		Total power used (mW):	221.74
		Assumed power supply efficiency:	0.85
		Total input power (mW):	**260.87**

[1] Assuming +3.3V rail is at maximum tolerance of +5%: VDD = 3.465V

[2] MCU datasheet states dynamic current is 0.5mA / MHz: 24MHz * 0.5mA/MHz = 12mA

[3] Inst. amp supply current given at Vin = Vs/2

[4] Op-amp supply current given as 14.5mA at Io = 0, 1ma extra is added represent output load

Figure 2. Overall power consumption estimate for data logger

The total input power is estimated to be 260.87mW. This analysis shows that the data logger stays within the target power consumption of 500mW.

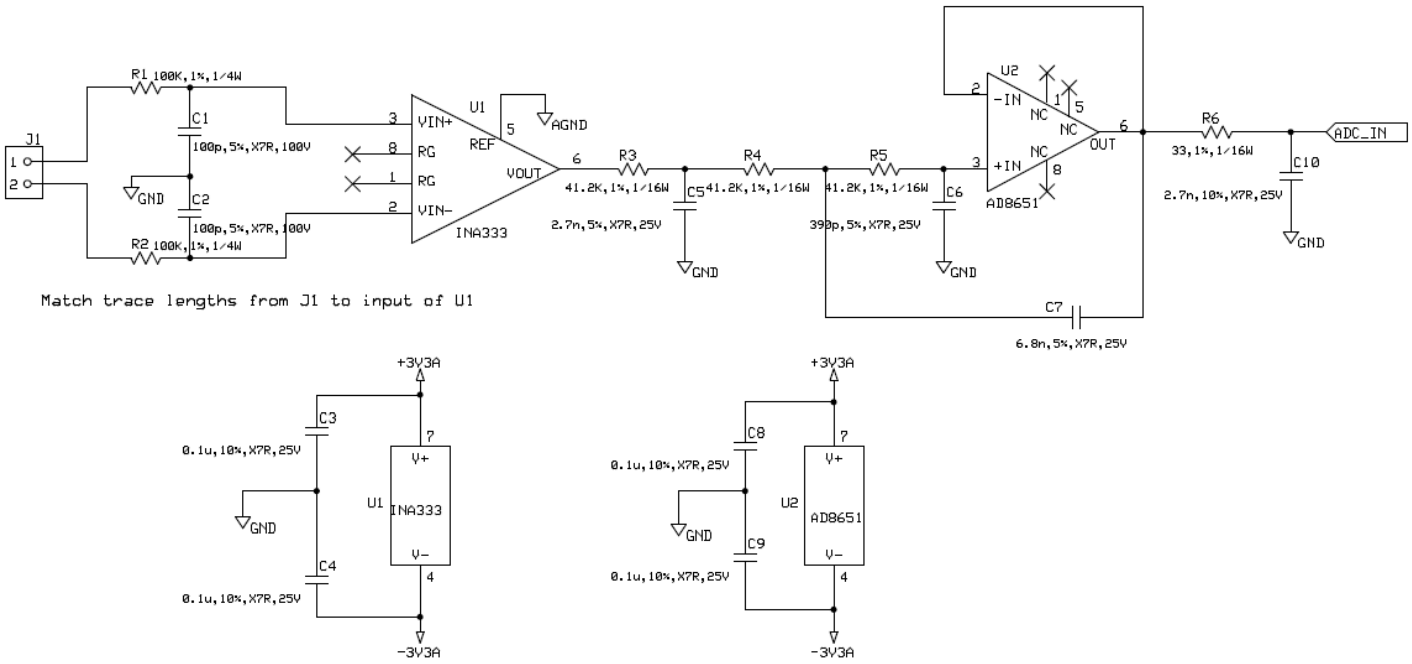
EMI protection:
The following measures are used to protect the data logger from electromagnetic interference on the power supply cable:

- Isolation to prevent noise on power cable from connecting directly to PCB ground plane
- Common-mode choke attenuates conducted noise
- MOV to clamp electrical surge events
- Filtering capacitors absorb and steer energy from electrical transients to chassis that are too fast to be clamped by the MOV

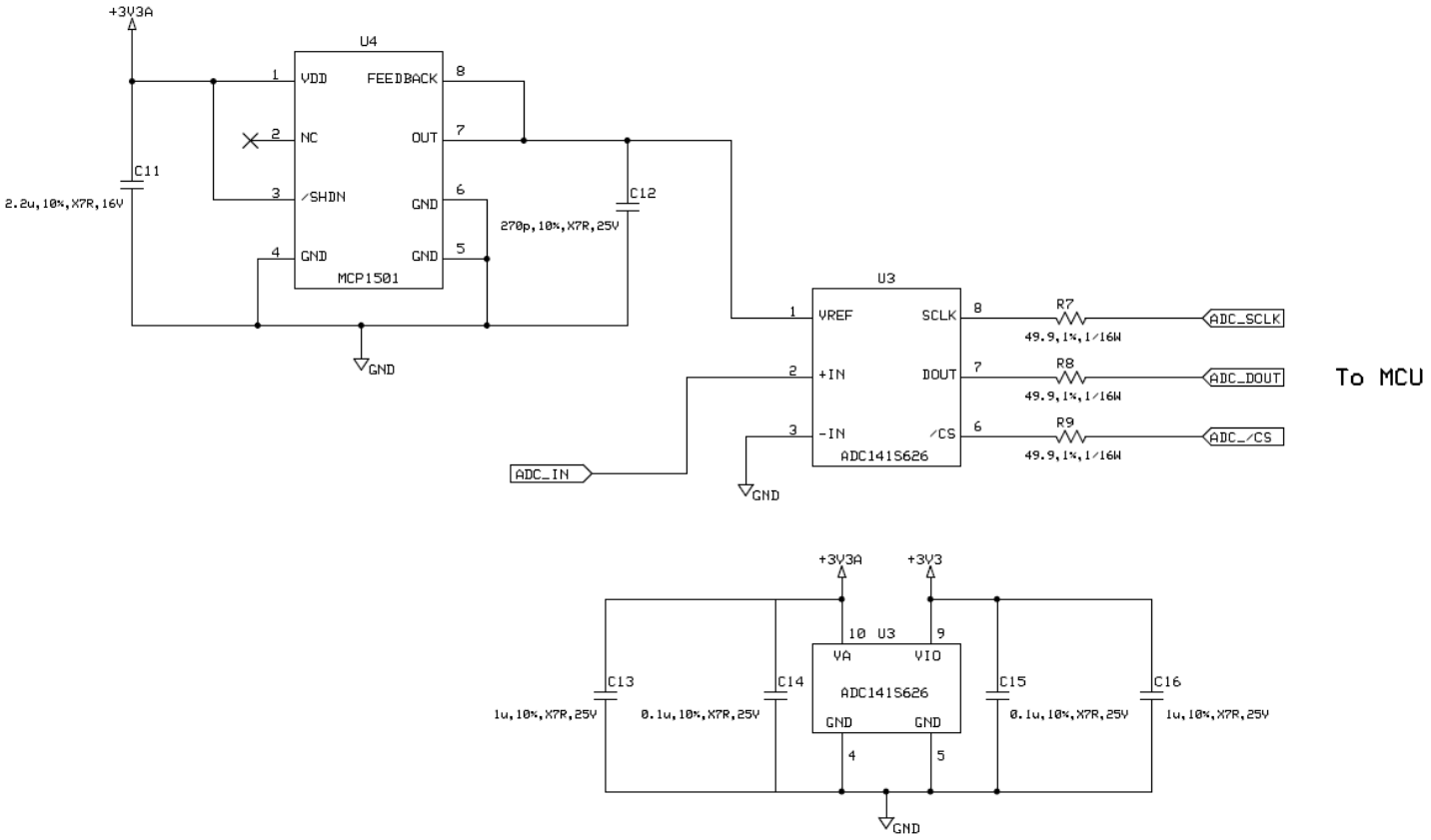
4. Analog Circuit

A. Schematic

The schematic and BOM for the analog inputs are shown below.



Schematic Sheet 1: EMI filtering, instrumentation amplifier, and anti-aliasing filter



Schematic Sheet 2: Voltage reference, ADC

Bill of Materials for analog circuit:

Part	Description	MFG Part Number
C1	100p,5%,X7R,100V	AVX 06031C101JAT2A
C2	100p,5%,X7R,100V	AVX 06031C101JAT2A
C3	0.1u,10%,X7R,25V	AVX 04023C103KAT2A
C4	0.1u,10%,X7R,25V	AVX 04023C103KAT2A
C5	2.7n,5%,X7R,25V	AVX 04023C272JAT2A
C6	390p,5%,X7R,25V	AVX 04023C391JAT2A
C7	6.8n,5%,X7R,25V	AVX 04023C391JAT2A
C8	0.1u,10%,X7R,25V	AVX 04023C103KAT2A
C9	0.1u,10%,X7R,25V	AVX 04023C103KAT2A
C10	2.7n,10%,X7R,25V	AVX 04023C272KAT2A
C11	2.2u,10%,X7R,16V	AVX 0603YC225KAT2A
C12	270p,10%,X7R,25V	AVX 04023C271KAT2A
C13	1u,10%,X7R,25V	AVX 06033C105KAT2A
C14	0.1u,10%,X7R,25V	AVX 04023C103KAT2A
C15	0.1u,10%,X7R,25V	AVX 04023C103KAT2A
C16	1u,10%,X7R,25V	AVX 06033C105KAT2A
R1	100K,1%,1/4W	Vishay CRCW1206100KFKEA
R2	100K,1%,1/4W	Vishay CRCW1206100KFKEA
R3	41.2K,1%,1/16W	Vishay CRCW040241K2FKED
R4	41.2K,1%,1/16W	Vishay CRCW040241K2FKED
R5	41.2K,1%,1/16W	Vishay CRCW040241K2FKED
R6	33,1%,1/16W	Vishay CRCW040233R0FKED
R7	49.9,1%,1/16W	Vishay CRCW040249R9FKED
R8	49.9,1%,1/16W	Vishay CRCW040249R9FKED
R9	49.9,1%,1/16W	Vishay CRCW040249R9FKED
U1	INA333	TI INA333AIDGKT
U2	AD8651	ADI AD8651ARZ
U3	ADC141S626	TI ADC141S626CIMM/NOPB
U4	MCP1501	Microchip MCP1501-10E/SN

B. Anti-Aliasing Filter Simulation

The anti-aliasing filter performance and stability is simulated in LTSpice. The simulation circuit is shown in Figure 3, and the gain/phase plot and the transient stability is shown in Figure 4.

An AC analysis shows the filter -3dB point occurs at 1.23kHz, which is close to the desired corner frequency of 1.2kHz. A 500Hz square wave is input to the filter to simulate the transient response, which can be used to estimate op-amp stability. The square wave experiences no ringing and has a somewhat slow response, indicating that the op-amp is in a stable configuration with high phase margin.

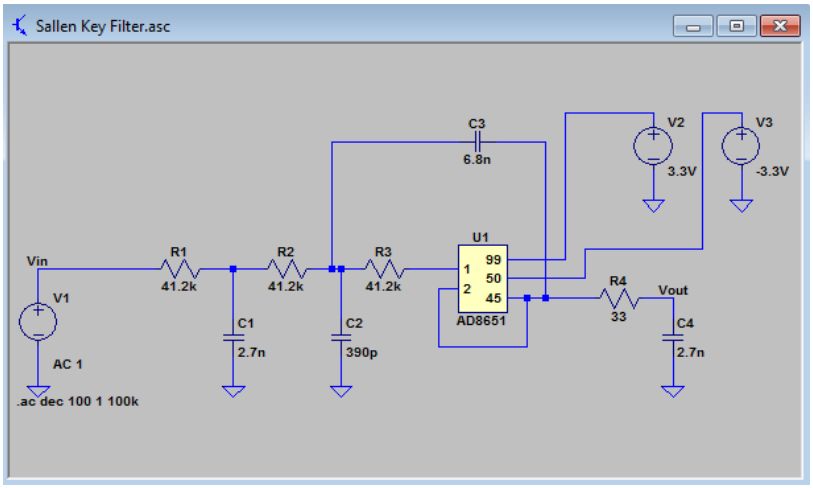


Figure 3. Anti-aliasing filter simulation using AD8651 SPICE model

Figure 4. Simulated gain/phase response (left), simulated step response transient stability (right)

5. PCB Layout

The proposed PCB layout for the data logger board is shown in Figure 5. Each component block in the figure is to scale; part dimensions were taken from datasheets of the selected parts. Components have not been selected for the power conversion circuits, so the Forward Converter Area in the figure shows the expected amount of area that will be taken by the power supply.

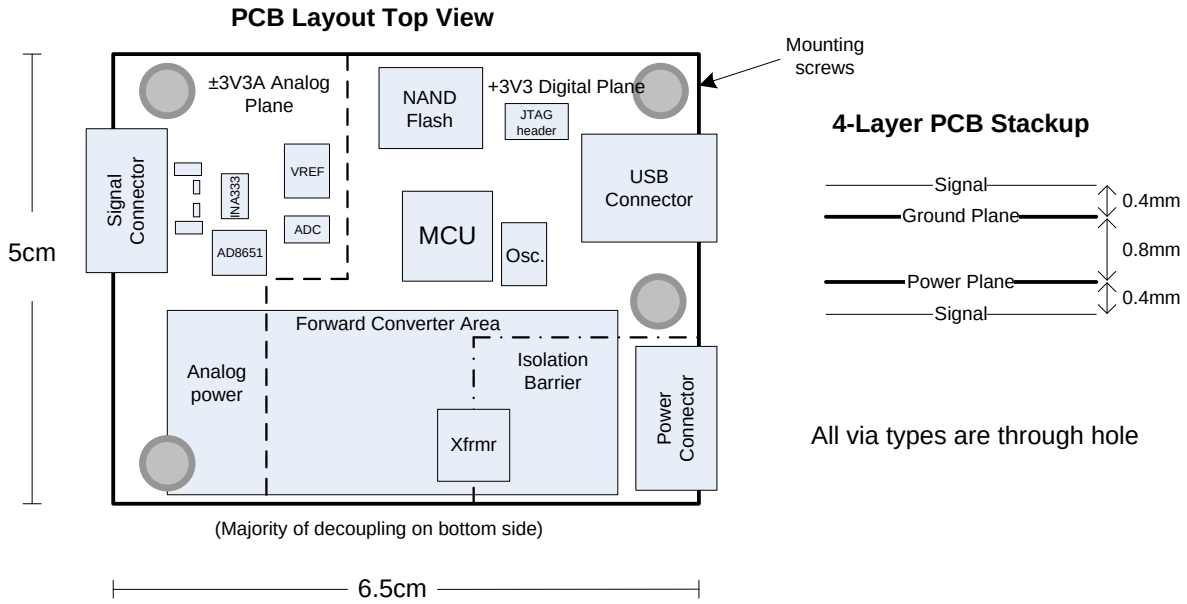


Figure 5. Proposed PCB layout. All component sizes are to scale

The layout is implemented on a 4-layer PCB that measures 5cm x 6.5cm. The proposed 4-layer stack up allows the signals to be tightly coupled to the ground and power planes, reducing current loop area. The following layout deliverables will be requested:

- Analog circuitry is kept separate from digital and power supply components
- Use a solid ground plane with as few slots and obstructions as possible
- Place decoupling capacitors to give as small of a current loop path as possible
- Route digital signals on one layer as much as possible, place decoupling capacitors by vias where signals travel from top to bottom layer
- Follow layout guidelines given by part datasheets

6. Test Plan

A. System-level Tests

System-level testing will be conducted to verify that the data logger meets the design requirements and to characterize its performance. These tests will be performed at -40°C, 25°C, and 85°C.

1. Apply a 500Hz, 1Vpp sine wave and run the data logger for 24 hours. Connect a USB device, download the acquired data, and verify that all 24 hours of waveform data is accurate.
2. Characterize data logger performance by applying various waveforms from 0Hz to 1.2kHz at magnitudes from 0.01Vpp to 1Vpp and storing several minutes' worth of data. Measure magnitude and phase shift relative to input signals to determine accuracy. Perform FFT on data and compare frequency plot to that of the input signals. Perform at -40°C, 25°C, and 85°C.
3. Allow the data logger to acquire data until its 2GB storage is filled (about 31.5 hours of data), and verify that it gracefully halts acquisition. Erase data and repeat multiple times to determine average length of time until storage is filled.

B. Circuit Functional Tests

Individual circuit blocks will be tested to characterize performance and to verify that components are operating within rated parameters.

Digital:

1. Measure a subset of signals in the NAND flash, ADC, and USB interfaces to verify that signal slew rates, overshoot, and undershoot are within datasheet parameters.
2. Measure critical timing parameters on NAND flash interface to determine how much data setup and hold time margin is available.

Analog:

1. Measure noise floor at input to ADC when instrumentation amplifier inputs are grounded.
2. Measure common mode rejection ratio of the analog input chain.
3. Measure input voltage at which ADC begins to saturate (output no longer changes with input)
4. Measure input impedance and verify it exceeds 1MΩ up to 1.2kHz.

Power supply:

1. For input voltages ranging from 15 -39V, load conditions ranging from no-load to 500mW, and at temperatures from -40°C to 85°C, perform the following:
    a. Verify 3.3V rail remains within ±5% tolerance
    b. Measure stress on critical components (such as MOSFET drain-source voltage) and verify they are within datasheet ratings
    c. Measure component temperatures and verify they do not exceed datasheet ratings
    d. Measure startup time
2. Verify overvoltage and undervoltage lockout protection is activated at the correct thresholds.
3. Verify power supply is able to handle power interruptions, brown-outs, and sudden shutdowns gracefully.
4. Verify isolation impedance exceeds 5MΩ at DC.

C. Electromagnetic Compatibility Tests

The data logger will be set up as it would in a typical use application (powered on, analog signal cables connected, USB unconnected, acquiring data) and subjected to various EMI and environmental tests. The data logger will be checked to verify it records and logs data with a specified accuracy during the EMI events.

Table 3 lists the tests, IEC standard describing the EMC test, and severity levels to be applied to the data logger.

Table 3 – EMC Tests

Test	Standard	Ports Applied To	Severity Level
Radiated Immunity	IEC 61000-4-3	Full product	10Vrms/m, 80MHz to 1GHz, 1.4GHz to 2.7GHz
Conducted Immunity	IEC 61000-4-6	Power supply, analog input	10Vrms, 0.15 to 80MHz
Electrostatic Discharge	IEC 61000-4-2	Power supply, analog input, USB input	±4kV peak
Surge Immunity	IEC 61000-4-5	Power supply	±1kV peak
Vibration	IEC 60255-21-1	Full product	10 – 150Hz, X - Y- Z directions, 2.0g acceleration

Appendix 1. Datasheets Referenced

Table 4 shows a list of the datasheets that were referenced for the parts used in this design.

Table 4 – Part Datasheets

Part	MFG P/N	Datasheet Revision
MCU	Microchip PIC32MX250F256H-I/PT	Rev D (APR 2016)
NAND flash	Micron MT29F16G16ADACAH4-IT	Rev N (APR 2014)
ADC	TI ADC141S626	MAR 2013
Op-amp	ADI AD8651ARMZ	Rev D (FEB 2014)
Inst. amp	TI INA333	DEC 2015
Reference voltage	Microchip MCP1501	Rev D (MAR 2017)